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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,399	03/23/2004	Masaru Kidoh	250892US2S	2347

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,399	KIDOH, MASARU	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 19-29* is/are pending in the application.

4a) Of the above claim(s) *8-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 19-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-7and 19-29 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The Rejections

Claims 1-7 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (U.S. 5,182,224).

Kim discloses a dynamic RAM structure with

(1) a semiconductor substrate (1);

a first insulation layer (12) formed on an inner surface of a trench formed in the semiconductor substrate (1) and having its top located above the surface of the semiconductor substrate (1);

a diffusion layer (14) formed within the semiconductor substrate (1), surrounding the deep portion of the trench (see Figure 1);

a first conductive layer (13) filled in the trench;

a gate electrode (8) provided on a gate insulation layer (10) formed on the surface of the semiconductor substrate (1);

source/drain diffusion layers (11) formed in the surface of the semiconductor substrate (1), sandwiching a channel region below the gate electrode (8);

a second conductive layer (7) extending on the first conductive layer (13), the first insulation layer (12), and one of the source/drain diffusion layers (11) (see Figure 1);

(2) wherein the first insulation layer is provided on the inner surface of the trench without exposing a side of the semiconductor substrate within the trench (see Figure 1);

(3) wherein the second conductive layer is provided without contacting the side of the semiconductor substrate (see Figure 1);

(4) wherein a top of the first conductive layer is located above the surface of the semiconductor substrate (see Figure 1);

(5) further comprising a second insulation layer overlying the top of the first insulation layer (see Figure 1);

(6) further comprising a third insulation layer provided on the first conductive layer and consisting of a same material of the first insulation layer (see column 6, lines 1-30);

(7) further comprising a device isolation insulation layer consisting of a same material as the first and third insulation layers and having in its surface a concave whose bottom is located above the surface of the semiconductor substrate (see Figure 1);

(19) wherein an end of the one of the source/drain diffusion layers on which the second conductive layer extends contacts a side of the first insulation layer (see Figure 1);

(20) wherein the second conductive layer electrically connects the first conductive layer to the one of the source/drain diffusion layers on which the second conductive layer extends (see Figure 1).

Claims 21-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Tadaki et al. (U.S. 5,349,218).

Tadaki discloses a semiconductor integrated circuit device with

(21) a semiconductor substrate (21);

a first insulation layer (32) formed on an inner surface of a trench formed in the semiconductor substrate (21) and having its top located above a surface of the semiconductor substrate (21);

a diffusion layer (30) formed within the semiconductor substrate (21), surrounding the deep portion of the trench;

a first conductive layer (33) filled in the trench;

a gate electrode (36G) provided on a gate insulation layer (35) formed on the surface of the semiconductor substrate (21), a bottom surface of the gate electrode being lower than a top surface of the first conductive layer (see Figure 2);

source/drain diffusion layers (SR) formed in the surface of the semiconductor substrate (21), sandwiching a channel region below the gate electrode (36G);

a second conductive layer (42) extending on the first conductive layer (33), the first insulation layer (32), and one of the source/drain diffusion layers (SR) (see Figure 2);

(22) wherein the first insulation layer is provided on the inner surface of the trench without exposing a side of the semiconductor substrate within the trench (see Figure 2);

(23) wherein the second conductive layer is provided without contacting the side of the semiconductor substrate (see Figure 2);

(24) wherein a top of the first conductive layer is located above the surface of the semiconductor substrate (see Figure 2);

(25) further comprising a second insulation layer overlying the top of the first insulation layer (see Figure 2);

(26) further comprising a third insulation layer provided on the first conductive layer and consisting of a same material of the first insulation layer (see Figure 2);

(27) further comprising a device isolation insulation layer consisting of a same material as the first and third insulation layers and having in its surface a concave

whose bottom is located above the surface of the semiconductor substrate (see Figure 2);

(28) wherein an end of the one of the source/drain diffusion layers on which the second conductive layer extends contacts a side of the first insulation layer (see Figure 2);

(29) wherein the second conductive layer electrically connects the first conductive layer to the one of the source/drain diffusion layers on which the second conductive layer extends (see Figure 2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
May 2, 2006